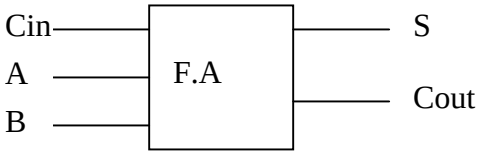
Answers Homework G51CSA- Digital Logic II

4)

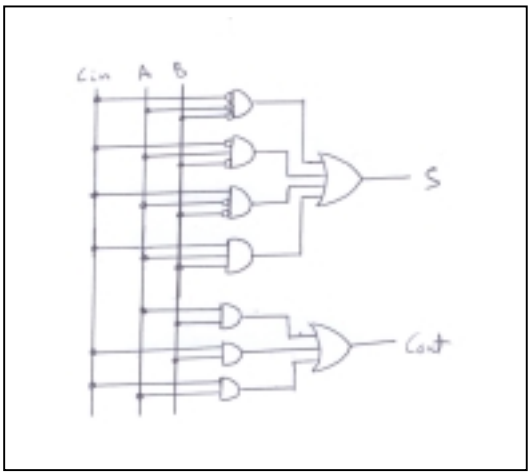


Cin	A	B	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Simplifying (for example using Karnaugh map) S and Cout we have:

$$S = \overline{Cin} \cdot \overline{A} \cdot \overline{B} + \overline{Cin} \cdot A \cdot \overline{B} + Cin \cdot \overline{A} \cdot \overline{B} + Cin \cdot A \cdot B$$

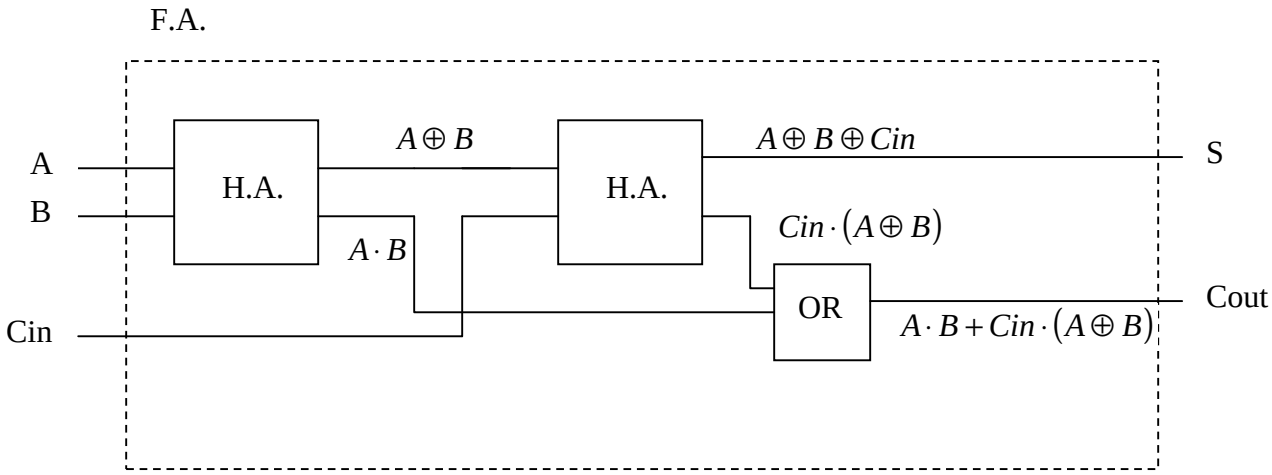
$$Cout = A \cdot B + Cin \cdot B + Cin \cdot A$$



5)

The first half adder operates the bits A and B and generates the sum of A and B and the carry.
The second half adder operates the result of the first half adder and the carry in, and generates the final sum and the carry out.

NOTE: $A \oplus B = A \cdot \overline{B} + \overline{A} \cdot B$



6)

A,B,C are the control inputs.
I0, I1, ... I7 are the data inputs.
Out is the output of the multiplexer.

A	B	C	Out
0	0	0	I0
0	0	1	I1
0	1	0	I2
0	1	1	I3
1	0	0	I4
1	0	1	I5
1	1	0	I6
1	1	1	I7

This truth table can be implemented in two stages of logic gates, AND-OR.

NOTE: The circles in the input of the AND gates stand for and inverter (a NOT gate).