SCHOOL OF COMPUTER SCIENCE AND INFORMATION TECHNOLOGY

G51CSA Homework problems – #VI

1. A set associative cache consists of 64 lines divided into four-line sets. Main memory contains 4k blocks of 128 words each. Show the format of main memory addresses.

2. A system has a byte addressable main memory of 16 Mbytes and a cache of 64k bytes. Data is transferred between main memory and cache in blocks of 4 bytes each. For the hexadecimal main memory addresses, 111111, 666666, BBBBBB, show the following information, in hexadecimal format:

   (a) Tag, line and word values for a direct mapped cache
   (b) Tag and word values for an associative cache
   (c) Tag, set and word values for a two-way set associative cache.

3. Consider a machine with a byte addressable main memory of 2^{16} bytes and block size of 8 bytes. Assume that a direct mapped cache consisting of 32 lines is used with this machine.

   (a) How many total bytes of memory can be stored in cache?
   (b) How is a 16-bit memory address divided into tag, line number, and byte number?
   (c) Into which line would bytes with each of the following addresses be stored?

   0001 0001 0001 1011
   1100 0011 0011 0100
   1101 0000 0001 1101
   1010 1010 1010 1010

   (d) Suppose the byte with address 001 1010 0001 1010 is stored in the cache. What are the addresses of the other bytes stored along with it?

4. Consider a 32-bit microprocessor that has an on chip 16-kbyte four-way set associative cache. Assume that the cache has a line size of four 32-bit words. Draw a block diagram of this cache, showing its organisation and how the different address fields are used to determine a cache miss/hit. Where in the cache is the word from memory location ABCDE8F8 mapped?

5. A computer system contains a main memory of 32K 16-bit words. It also has a 4K-word cache divided into four-line sets with 64 words per line. Assume that the cache is initially empty. The processor fetches words from locations 0, 1, 2, 3, …, 4350, 4351 in that order. It then repeats this fetch sequence nine more times. The cache is 10 times faster than main memory. Estimate the improvement resulting from the use of the cache. Assume an LUR policy for block replacement.